CLAIMS

What is claimed is:

1. A semiconductor device for use in a stacked multi-chip assembly, comprising:

a semiconductor die; and

a spacer layer formed on at least a portion of a surface of said semiconductor die and protruding therefrom substantially a predetermined distance that said semiconductor die and an adjacent semiconductor die of said stacked multi-chip assembly are to be spaced apart from one another, said spacer layer including voids communicating with a lateral periphery thereof.

2. The semiconductor device of claim 1, wherein said spacer layer comprises a plurality of laterally discrete spacers.

3. The semiconductor device of claim 1, further comprising:

at least one discrete conductive element protruding above a surface of said semiconductor die.

4. The semiconductor device of claim 3, wherein said at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. The semiconductor device of claim 1, wherein said predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

6. The semiconductor device of claim 1, wherein said predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

7. The semiconductor device of claim 1, wherein said spacer layer covers only a portion of said surface.

8. The semiconductor device of claim 7, wherein said spacer layer comprises a pattern.

9. The semiconductor device of claim 7, wherein said spacer layer comprises randomly arranged features.

10. The semiconductor device of claim 1, wherein said spacer layer comprises a material that will adhere to a surface of said adjacent semiconductor die.

11. The semiconductor device of claim 1, wherein said spacer layer comprises a polymer.

12. The semiconductor device of claim 11, wherein said polymer comprises a photoimageable polymer.

13. The semiconductor device of claim 1, wherein said spacer layer comprises at least one of a glass, a silicon dioxide, a silicon nitride, and a silicon oxynitride.

14. The semiconductor device of claim 1, wherein said spacer layer is positioned on an active surface of said semiconductor die.

15. The semiconductor device of claim 1, wherein said spacer layer is positioned on a back side of said semiconductor die.

16. The semiconductor device of claim 1, further comprising:
another spacer layer covering at least a portion of an opposite surface of said semiconductor die.

17. The semiconductor device of claim 1, further comprising:
adhesive material on an exposed surface of said spacer layer.

18. The semiconductor device of claim 1, wherein said spacer layer comprises a plurality of at least partially superimposed, contiguous, adhered sublayers.

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19. A semiconductor device assembly, comprising:
a first semiconductor device;
a nonconfluent spacer layer on a surface of said first semiconductor device; and
a second semiconductor device positioned over said first semiconductor device, a surface of said second semiconductor device being adhered to said nonconfluent spacer layer.

20. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of said nonconfluent spacer layer.

21. The semiconductor device assembly of claim 20, wherein said at least one void facilitates lateral introduction of adhesive material between said first and second semiconductor devices.

22. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer has a substantially uniform thickness.

24. The semiconductor device assembly of claim 19, further comprising:

at least one discrete conductive element protruding above a surface of at least one of said first and second semiconductor devices and located at least partially between said first and second semiconductor devices.

25. The semiconductor device assembly of claim 24, wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that exceeds a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

26. The semiconductor device assembly of claim 24, wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that is about the same as or less than a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

27. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises dielectric material.

28. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a polymer.

29. The semiconductor device assembly of claim 28, wherein said polymer adheres to surfaces of said first semiconductor device and said second semiconductor device.

30. The semiconductor device assembly of claim 28, wherein said polymer comprises a photoimageable polymer.

31. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered sublayers.

32. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

33. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a pattern.

34. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises randomly arranged features.

35. The semiconductor device assembly of claim 19, further comprising:
an adhesive material securing said nonconfluent spacer layer to at least one of said surface of said first semiconductor device and said surface of said second semiconductor device.

36. The semiconductor device assembly of claim 35, wherein said adhesive material is located within voids in said nonconfluent spacer layer.

37. The semiconductor device assembly of claim 19, further comprising:
a substrate upon which one of said first semiconductor device and said second semiconductor device is positioned.

38. The semiconductor device assembly of claim 37, wherein at least one bond pad of at least one of said first semiconductor device and said second semiconductor device is in communication with a corresponding contact area of said substrate.

39. The semiconductor device assembly of claim 37, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

40. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer is positioned between an active surface of said first semiconductor device and a back side of said second semiconductor device.

41. The semiconductor device assembly of claim 19, further comprising:
at least one additional semiconductor device.

42. The semiconductor device assembly of claim 19, further comprising:
a plurality of nonconfluent spacer layers between said first and second semiconductor devices, additive thicknesses of said plurality of nonconfluent spacer layers defining a distance said first and second semiconductor devices are spaced apart from one another.

43. The semiconductor device assembly of claim 42, wherein a first nonconfluent spacer layer of said plurality of nonconfluent spacer layers is secured to a surface of said first semiconductor device and a second nonconfluent spacer layer of said plurality of nonconfluent spacer layers is secured to an opposed surface of said second semiconductor device.

44. The semiconductor device assembly of claim 42, wherein at least some solid regions of each of said plurality of nonconfluent spacer layers are at least partially superimposed relative to one another.

45. A multi-chip module, comprising:

a substrate;

a first semiconductor device positioned on said substrate;

a nonconfluent layer comprising dielectric material over said first semiconductor device;

a second semiconductor device positioned over said nonconfluent layer; and

an encapsulant covering at least portions of said first semiconductor device, said nonconfluent layer, said second semiconductor device, and portions of said substrate located adjacent said first semiconductor device.

46. The multi-chip module of claim 45, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

47. The multi-chip module of claim 45, wherein at least one bond pad of at least one of said first semiconductor device and said second semiconductor device is in electrical communication with a corresponding contact area of said substrate.

48. The multi-chip module of claim 47, wherein said electrical communication is established by at least one discrete conductive element extending at least partially between said first and second semiconductor devices and protruding above a surface of at least one of said first semiconductor device and said second semiconductor device.

49. The multi-chip module of claim 48, wherein said nonconfluent layer has a thickness that exceeds a distance said at least one discrete conductive element protrudes above said surface.

50. The multi-chip module of claim 48, wherein a thickness of said nonconfluent layer is about the same as or less than a distance said at least one discrete conductive element protrudes above said surface.

51. The multi-chip module of claim 45, wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

52. The multi-chip module of claim 45, wherein said nonconfluent layer comprises a pattern.

53. The multi-chip module of claim 45, wherein said nonconfluent layer comprises randomly arranged features.

54. The multi-chip module of claim 45, wherein said nonconfluent layer has a substantially consistent height.

55. The multi-chip module of claim 45, wherein said nonconfluent layer comprises a dielectric material.

56. The multi-chip module of claim 55, wherein said dielectric material comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

57. The multi-chip module of claim 45, wherein said nonconfluent layer comprises a polymer.

58. The multi-chip module of claim 57, wherein said polymer is capable of adhering to a surface of at least one of said first semiconductor device and said second semiconductor device.

59. The multi-chip module of claim 57, wherein said polymer comprises a photoimageable polymer.

60. The multi-chip module of claim 45, wherein said nonconfluent layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered layers.

61. The multi-chip module of claim 45, further comprising:
an adhesive material securing said first and second semiconductor devices to one another.

62. The multi-chip module of claim 61, wherein said adhesive material is located within voids of said nonconfluent layer.

63. The multi-chip module of claim 45, wherein said encapsulant comprises a glob-top type encapsulant.

64. The multi-chip module of claim 45, wherein said encapsulant comprises a molded encapsulant.

65. The multi-chip module of claim 45, further comprising:
a plurality of nonconfluent layers between said first and second semiconductor devices, additive thicknesses of said plurality of nonconfluent layers defining a distance said first and second semiconductor devices are spaced apart from one another.

66. The multi-chip module of claim 65, wherein a first nonconfluent layer of said plurality of nonconfluent layers is secured to a surface of said first semiconductor device and a second nonconfluent layer of said plurality of nonconfluent layers is secured to an opposed surface of said second semiconductor device.

67. The multi-chip module of claim 65, wherein at least some solid regions of each of said plurality of nonconfluent layers are at least partially superimposed relative to one another.

68. A method for preparing a semiconductor device to be used in a multi-chip module, comprising:
providing at least one semiconductor device; and

forming at least one nonconfluent spacer layer on at least one surface of said at least one semiconductor device.

69. The method of claim 68, wherein said forming comprises forming nonconfluent spacer layers on both surfaces of said at least one semiconductor device.

70. The method of claim 68, wherein said forming comprises screen printing.

71. The method of claim 68, wherein said forming comprises:
forming a material layer on said at least one surface; and
patterning said material layer.

72. The method of claim 71, wherein said forming said material layer comprises depositing said material layer.

73. The method of claim 71, wherein said patterning comprises:
forming a mask over said material layer; and
removing portions of said material layer exposed through said mask.

74. The method of claim 68, wherein said forming comprises stereolithographically forming said at least one nonconfluent spacer layer.

75. The method of claim 74, wherein said stereolithographically forming comprises:
forming a layer comprising unconsolidated material over said at least one surface; and
at least partially consolidating selected portions of said layer.

76. The method of claim 75, further comprising:

forming at least one additional layer comprising unconsolidated material over said layer; and

at least partially consolidating selected portions of said at least one additional layer, said at least partially consolidated portions of said another layer being at least partially superimposed over, contiguous with, and adhered to said at least partially consolidated portions of said layer.

77. The method of claim 76, further comprising:

repeating said forming and said at least partially consolidating at least once.

78. A method for designing a semiconductor device to be used in a stacked multi-chip module, comprising:

configuring at least one nonconfluent spacer layer to be positioned on at least one surface of the semiconductor device.

79. The method of claim 78, wherein said configuring comprises configuring said at least one nonconfluent spacer layer with at least one void to facilitate lateral introduction of adhesive material through said at least one nonconfluent spacer layer onto said at least one surface of the semiconductor device.

80. The method of claim 78, wherein said configuring comprises configuring said at least one nonconfluent spacer layer to have a thickness that exceeds a distance at least one discrete conductive element will protrude above a surface of at least one of the semiconductor device and another, adjacent semiconductor device of the multi-chip module.

81. The method of claim 78, wherein said configuring comprises configuring said at least one nonconfluent spacer layer to have a thickness that is about the same as or less than a distance at least one discrete conductive element will protrude above a surface of at least one of the semiconductor device and another, adjacent semiconductor device of the multi-chip module.

82. The method of claim 78, wherein said configuring comprises configuring said at least one nonconfluent spacer layer to include a plurality of laterally discrete spacers.

83. The method of claim 78, wherein said configuring comprises configuring said at least one nonconfluent spacer layer to be positioned adjacent another spacer layer, said at least one nonconfluent spacer layer and said another spacer layer together defining a distance the semiconductor device is to be spaced apart from another, adjacent semiconductor device of the multi-chip module.

84. A method for forming a stacked assembly of semiconductor devices, comprising:
providing a first semiconductor device;
applying a nonconfluent spacer layer to at least one surface of said first semiconductor device; and
positioning a second semiconductor device in stacked arrangement relative to said first semiconductor device, said nonconfluent spacer layer at least partially spacing said first and second semiconductor devices apart from one another.

85. The method of claim 84, further comprising:
securing said first semiconductor device and a substrate to one another.

86. The method of claim 85, wherein said securing comprises securing a back side of said first semiconductor device to said substrate.

87. The method of claim 85, wherein said securing comprises securing said substrate to portions of an active surface of said first semiconductor device.

88. The method of claim 85, further comprising:
electrically connecting at least one bond pad of said first semiconductor device to a corresponding contact area of said substrate.

89. The method of claim 88, wherein said electrically connecting comprises positioning or forming a discrete conductive element between said at least one bond pad and said corresponding contact area.

90. The method of claim 88, wherein said electrically connecting comprises placing a lead at least partially over said at least one bond pad.

91. The method of claim 85, wherein said applying is effected before said securing.

92. The method of claim 85, wherein said applying is effected after said securing.

93. The method of claim 88, wherein said applying is effected after said electrically connecting.

94. The method of claim 84, further comprising:

applying another nonconfluent spacer layer to at least one surface of said second semiconductor device.

95. The method of claim 94, wherein, upon said positioning, said nonconfluent spacer layer and said another nonconfluent spacer layer are positioned against one another.

96. The method of claim 84, wherein, upon said positioning, said nonconfluent spacer layer adheres said first and second semiconductor devices to one another.

97. The method of claim 84, further comprising:

laterally introducing adhesive material into voids in said nonconfluent spacer layer and between said first and second semiconductor devices.

98. The method of claim 97, further comprising at least one of at least partially curing and at least partially hardening said adhesive material.

99. The method of claim 88, further comprising:

electrically connecting at least one bond pad of said second semiconductor device to another corresponding contact area of said substrate.

100. The method of claim 99, further comprising:

encapsulating at least portions of said first semiconductor device, said second semiconductor device, and said substrate.

101. The method of claim 100, wherein said encapsulating comprises forming a molded encapsulant.

102. The method of claim 100, wherein said encapsulating comprises forming a glob-top encapsulant.